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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,668	03/29/2004	Kenji Ichikawa	SAT 200	1142

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,668	ICHIKAWA, KENJI	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3 and 5-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3 and 5-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 24 May 2006 has been entered.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: "a gate connected to a first-conductivity-type layer under a gate of said second-conductivity-type MOS output transistor", there is no drawing or figure that shows a gate of the second conductivity type MOS output transistor connected to a first conductivity type layer under a gate of said second conductivity-type MOS output transistor.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 5, 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6885529 to Ker et al.

Regarding claim 32, Ker discloses in fig. 9 a semiconductor apparatus comprising: an output electrode 60 from which an output signal of the semiconductor apparatus is output; a first-conductivity-type (N type) MOS output transistor Mn6, col. 5 line 49, respectively including a drain electrode connected to the output electrode, fig. 9, a source electrode connected to a ground voltage terminal (Vss_I/O), a gate electrode connected to a signal line (pre-buffer), and a second-conductivity type (P-type) layer 84, located under the gate electrode, fig. 10, wherein the first conductivity type MOS output transistor Mn6 transmits the output signal of the semiconductor apparatus to the output electrode 60 responsive to a signal on the signal line (pre-buffer); a first conductivity type (N) MOS protection transistor Mn7, col. 5 line 51, respectively including a drain electrode connected to the output electrode 60, a source electrode connected to the ground voltage terminal (Vss_I/O), and a gate electrode connected to the ground voltage terminal, fig. 9; and a metallic wiring member (the wire between S/D of Mn6 connecting to Vss_I/O and gate of Mn7) which connects the second conductivity type layer of the first conductivity type MOS output transistor Mn6 to the gate electrode of the first conductivity type MOS protection transistor Mn7, fig. 9.

Regarding claim 5, Ker discloses the semiconductor apparatus wherein the drain of said first-conductivity-type MOS protection transistor Mn7 is formed closer to the output electrode 60 than the drain of said first-conductivity-type MOS output transistor Mn6, fig. 9.

Regarding claim 31, Ker discloses the semiconductor apparatus wherein the gate of said first-conductivity-type MOS protection transistor Mn7 is directly connected by the electrode wiring to said second conductivity type layer 84 under the gate of first conductivity type MOS output transistor Mn6, fig. 9.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-3, 6-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6885529 to Ker et al. in view of US 5610790 to Staab et al.

Regarding claims 2, 7, 11 and 14, Ker does not disclose the semiconductor apparatus wherein said first-conductivity-type MOS output transistor m10 and said first-conductivity-type MOS protection transistor m11 are of an SOI structure.

However, Staab discloses the semiconductor apparatus in fig. 7-8a a protection circuit 700 comprises first-conductivity-type MOS output transistor 722, column 6 line 67, and said first-conductivity-type MOS protection transistor 716,

column 7 line 4, are of an SOI structure, fig 8a column 6 line 45. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the SOI substrate teaching of Staab with Ker's device, because it would have increased the device speed as taught by Staab, see abstract.

Regarding claim 3, 8, 12, and 15, Ker discloses the semiconductor apparatus comprising: a second-conductivity-type area P+, fig. 10, connected to said second-conductivity-type layer 84 under the gate electrode of said first-conductivity-type MOS output transistor Mn6, wherein the gate electrode of said first-conductivity-type MOS protection transistor Mn7 is connected via said second-conductivity-type area P+ to said second-conductivity-type layer 84 under the gate electrode of said first-conductivity-type MOS output transistor Mn6, fig. 9.

Regarding claims 6, 21, Ker does not disclose the semiconductor apparatus wherein said first-conductivity-type MOS protection transistor Mn7 is higher in electrostatic destruction withstand voltage than said first-conductivity-type MOS output transistor Mn6.

However, Ker discloses the structure in fig. 9 is substantially or identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claims 9 and 13, Ker discloses the semiconductor apparatus wherein the gate electrode of said first-conductivity-type MOS protection transistor Mm7 is connected by an electrode wiring to said second-conductivity-type layer 84 under the gate of said first-conductivity-type MOS output transistor Mm6, fig. 9.

Regarding claim 10, Ker discloses the semiconductor apparatus wherein the drain of said first-conductivity-type MOS protection transistor Mm7 is formed closer to the output electrode 60 than the drain of said first-conductivity-type MOS output transistor Mm6, fig. 9.

Regarding claim16, Ker discloses a semiconductor apparatus, which protects a first conductivity type (N) MOS output transistor Mn6 and a second conductivity type (P) MOS output transistor Mp6, col. 5 line 23, against a surge entering through an output electrode 60 connected to each of drains of said first conductivity type MOS output transistor Mn6 whose source is connected to ground Vss_I/O and said second conductivity type MOS output transistor whose source is connected to a power supply Vdd_I/O, fig. 9, said apparatus comprising: a first conductivity type MOS protection transistor Mn7 having a drain connected to the drain of said first conductivity type MOS output transistor Mn6, a source connected to a source of said first conductivity type MOS output transistor Mn6, and a gate connected to a second conductivity type layer 84 under a gate of said first conductivity type MOS output transistor Mn6, fig. 9; and a second conductivity type MOS protection transistor Mp7 having a drain connected to the drain of said second conductivity type MOS output transistor Mp6, a source

connected to a source of said second conductivity type MOS output transistor Mp6, fig. 9.

But, Ker does not expressly discloses a gate of the second conductivity type (P) MOS protection transistor Mp7 connected to a first conductivity type (N) layer under a gate of said second-conductivity type MOS output transistor Mp6. However, Ker show the gate of Mp7 connected to the substrate and it is typical CMOS structure where NMOS is formed on a P-well or P-substrate and PMOS is formed on a N-well or N-substrate, such typical CMOS structure is disclosed by US 6784496 (Brodsky) in fig. 4C. Thus, at the time the invention was made; it would have been obvious to one of ordinary skill in the art to understood from the teaching of Ker that the gate electrode of second conductivity type MOS protection Mp7 is connected to a first conductivity type (N) layer and that a PMOS transistor would have an opposite conductivity as disclosed in fig. 10.

Regarding claims 17, 22, 26, 29, Kerr does not discloses disclose the semiconductor apparatus wherein said first conductivity type MOS output transistor Mn6, said first conductivity type MOS protection transistor Mn7, said second conductivity type MOS output transistor Mp6 and said second-conductivity-type MOS protection transistor are of an SOI structure.

However, Staab discloses the semiconductor apparatus in fig. 7-8a a protection circuit 700 comprises first-conductivity-type MOS output transistor 722, column 6 line 67, and said first-conductivity-type MOS protection transistor 716, column 7 line 4, are of an SOI structure, fig 8a column 6 line 45. At the time the

invention was made; it would have been obvious to one of ordinary skill in the art to use the SOI substrate teaching of Staab with Ker's device, because it would have increased the device speed as taught by Staab, see abstract.

Regarding claims 18, 23, 27, 30, Ker discloses the semiconductor apparatus comprising: a second-conductivity type area P+, fig. 10, connected to said second-conductivity-type layer 84 under the gate of said first-conductivity type MOS output transistor Mn6;, wherein the gate of said first-conductivity-type MOS protection transistor Mn7 is connected via said second-conductivity-type area P+ to said second-conductivity type layer 84 under the gate of said first-conductivity type MOS output transistor Mn6.

With respect to "a first conductivity type area connected to said first-conductivity layer under the gate of said second-conductivity-type MOS output transistor Mp6 and wherein the gate of said second-conductivity-type MOS protection transistor Mp7 is connected via said first-conductivity-type area to said first-conductivity type layer under the gate of said second-conductivity type MOS output transistor Mp6", as discussed in the above claim 16, a typical PMOS structure would have an opposite conductivity as disclosed in fig. 10.

Regarding claims 19, 24, 28, Ker discloses the semiconductor apparatus wherein the gates of said first-conductivity-type MOS protection transistor Mn7 and said second-conductivity-type MOS protection transistor Mp7 are connected by electrode wirings respectively to said second-conductivity type layer 84 under the gate of said first-conductivity-type MOS output transistor Mn6 and to said first-conductivity layer under

the gate of said second-conductivity-type MOS output transistor Mp6 (see discussion in claim 16).

Regarding claims 20, 25, Ker discloses the semiconductor apparatus wherein the drain of said first-conductivity type MOS protection transistor Mn7 and said second-conductivity-type MOS protection transistor Mp7 are formed closer to the output electrode 60 than the drains of said first-conductivity-type MOS output transistor Mn6 and said second-conductivity type MOS output transistor Mp7, fig. 9.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
19 June 2006